ITRS - Yield Enhancement Working Group Update

Conference in Grenoble, France
October 07, 2014

Richard Oechsner, Lothar Pfitzner

lothar.pfitzner@iisb.fraunhofer.de
richard.oechsner@iisb.fraunhofer.de
Scope of Yield Enhancement

• **Aspects**
  - Manufacturing of integrated semiconductor devices: numerous processing steps building the 3D structure of the chip (e.g. 9 Cu and low-k interconnect layers for 32 nm)
  - Yield: percentage of operating chips at the end of the manufacturing process

• **Components**
  - Determination and control of contamination
  - Inspection of structures and critical dimensions
  - Model to predict and calculate yield based on historic contamination levels (particulate and metals) and defects (failures)
  - Determination of kill ratios: Correlation between defects and yield

**Gordon Moore:** “There is no fundamental obstacle to achieving device yields of 100%.”

*(Electronics, 38 (8), 1965)*
Defects and Failure Mechanisms

- processes: litho, etch thin film implantation, planarization, cleaning,…
- faults and problems: defects as e.g. particles, flatness, layer properties, patterns, dimensions
- challenges
  - yield and defect map in 2 D
  - root cause analysis requires 3 D
  - requires fast and non-destructive inspection (defect density) and metrology (root cause analysis) for 2D and 3D structures → CIA
  - requires preventive defect and contamination control → WECC
  - model, predict and forecast yield

Si crystal: stacking faults, contamination, stress, COP (crystal originating particles), epi defects

International Technology Roadmap for Semiconductors

Grenoble, October 7, 2014
Example: Inspection for ‘More than Moore’

Applications

‘More Moore’

and

‘More than Moore’ technologies

- power electronics
- mechatronics
- MEMS applications
- packaging and assembly
- 3D integration

Laboratory scale inspection setup fulfilling requirements of low cost components and large area inspection (4 mm * 4 mm field of view at µm resolution) (example for 3D integration, EC & BMBF funded project JEMSIP3D under contract ENIAC Call 2008/120016)
Contamination Analysis for Manufacturing Control

• Drivers
  – ultra clean manufacturing
  – unintended contamination of layers
  – dimensional, structural and compositional information
  – depth resolved quantification
  – non-volatile organic surface contamination

• Analytical Techniques for Manufacturing Control
  – x-ray metrology
  – GCMS

For metals, Grazing Incidence X-Ray Fluorescence (GIXRF) could be a possible solution providing dimensional quantification and qualification of surface near elemental contamination.
Objectives of Yield Enhancement

• **collect defect data**
  – tools for inspection and root cause analysis
  – automated defect classification and filtering
  – inspection strategy

• **yield management**
  – software
  – objective: to correlate data and find excursions
  – predict yield

• **defect data excursions**
  – define specs
  – procedure for clarification

[Diagram showing the processes and modules involving wafer inspection and collection of data, defect classification, and defect densities.]

**International Technology Roadmap for Semiconductors**

Grenoble, October 7, 2014
### YE ITWG Contributors

#### Europe
- **Lothar Pfitzner** (YE chair, Fraunhofer IISB)
- **Andreas Neuber** (WECC chair, AMAT)
- **Sabrina Anger** (CIA, Fraunhofer IISB)
- **Yannick Borde** (WECC AMC, ST Crolles)
- **Richard Bruls** (WECC UPW, ASML)
- **Jan Cavelaars** (CIA, NXP)
- **Arnaud Favre** (WECC AMC, adixen Vacuum Products)
- **Giuseppe Fazio** (Micron)
- **Astrid Gettel** (WECC AMC co-chair, GF)
- **Mathias Haeuser** (CIA, Infineon)
- **Fontaine Herve** (WECC AMC, CEA leti)
- **Christoph Hocke** (WECC AMC, Infineon Technologies)
- **Jost Kames** (WECC AMC, artemis control AG)
- **Barry Kennedy** (CIA, Intel)
- **Andreas Nutsch** (CIA, PTB)
- **Dieter Rathei** (CIA, DR Yield)
- **Ines Thurner** (CIA, CONVANIT)
- **Hubert Winzig** (WECC, Infineon)

#### Singapore
- **Guillaume Gallet** (WECC AMC, Camfil)
- **Paul Tan** (WECC)

#### Taiwan
- **Wai-Ming Choi** (Entegris)
- **Yuchuang Huang** (TSMC)
- **Victor Liang** (TSMC)
- **Ray Yang** (UMC)
- **Mao-Hsiang Yen** (Winbond)

#### Japan
- **Takashi Futatsuki** (WECC UPW, Organo)
- **Misako Saito** (WECC, TEL)
- **Masahiko Ikeno** (CIA, Hitachi High-Technologies)
- **Katsunobu Kitami** (WECC, Kurita)
- **Koichiro Saga** (WECC CIA, SONY)
- **Isamu Sugiyama** (WECC, NOMURA)
- **Makiko Tamaoki** (WECC, Toshiba)
- **Takashi Tsuchiya** (CIA, Fujitsu semiconductor)

#### Korea
- **Yoshimi Shiramizu** (WECC, co-chair, Samsung)
- **Young Jeong Kim** (CIA, Samsung)

### Thank you very much!

#### United States
- **Scott Anderson** (WECC, Balazs-AirLiquide)
- **Dwight Beal** (WECC, PMS)
- **David Blackford** (WECC UPW, Fluid Measurement Technologies)
- **Dilip Patel** (YE co-chair, ISMI)
- **Mark Camenzind** (WECC, Balazs-AirLiquide)
- **Hubert Chu** (WECC, AMAT)
- **Robert Clark** (WECC, TEL)
- **Jeff Covington** (WECC UPW, Freescale)
- **John DeGenova** (WECC AMC, Texas Instruments)
- **Charley Dobson** (WECC, TI)
- **Dan Fuchs** (WECC, Air Liquide)
- **Rick Godec** (WECC UPW, Ionics Instruments)
- **Milton Goldwin** (CIA, ISMI)
- **Barry Gotlinsky** (WECC UPW, Pall)
- **Asad Haider** (WECC, TI)
- **Jeff Hanson** (WECC UPW, Texas Instruments)
- **Keith Kerwin** (WECC, TI)
- **Suhas Ketkar** (WECC, APCI)
- **Alan Knapp** (WECC UPW, Siemens WT)
- **John Kurowski** (WECC, IBM)
- **Bob Latimer** (WECC, Hach)
- **Ravi Laxman** (WECC, Air Liquide)
- **Slava Libman** (WECC UPW co-chair, Balazs Nanoanalysis)
- **Rushi Matkar** (WECC UPW, Intel)
- **Tim Miller** (WECC UPW, Purdue)
- **William Moore** (WECC, IBM)
- **Chris Muller** (WECC AMC, Purafil, Inc.)
- **Jim Ohsen** (WECC, Entegris)
- **Ruben Pessina** (WECC, TI)
- **Larry Rabellino** (WECC, SAES)
- **Rich Riley** (WECC UPW, Intel)
- **David Roberts** (WECC, Nantero)
- **Biswanath Roy** (WECC, Pall)
- **Tony Schleisman** (WECC, Air Liquide)
- **Drew Sinha** (WECC UPW, Siltronic)
- **Jim Snow** (WECC UPW, DNS)
- **Terry Stange** (WECC UPW, Hach Ultra Analytics)
- **Dan Wilcox** (WECC UPW co-chair, Spansion)
- **Bernie Zerfas** (WECC UPW, IBM)

---

**Status 12/2013**

**International Technology Roadmap for Semiconductors**

Grenoble, October 7, 2014
2014 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- **Near Term (2014-2018)**
  - *Detection and Identification of Small Yield Limiting Defects from Nuisance* - It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high throughput. Furthermore, it is a dare to identify yield relevant defects under a vast amount of nuisance and false defects.

  - *Process Stability vs. Absolute Contamination Level* – This includes the correlation to yield test structures, methods and data that are needed for correlating defects caused by wafer environment and handling to yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.

  - *Detection of organic contamination on surfaces* – The detection and speciation of nonvolatile organics on surfaces is currently not possible in the fab. There is no laboratory scale instrumentation available.

  - *Correlation of contamination level to yield*
2014 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- **Long Term (2019-2026)**
  - **Next Generation Inspection** - As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This assessment should include each technique’s ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.

  - **In-line Defect Characterization and Analysis** – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

  - **Next generation lithography** - Manufacturing faces several choices of lithography technologies in the long term, which all pose different challenges with regard to yield enhancement, defect and contamination control.
Overall YE activities

• Activities performed in 2013/2014:
  – Summary text for Executive Overview
  → 2013 revision of the YE ITRS roadmap chapter
  → Discussion of extended collaboration with selected ITWs
  – Review and update of tables
    • Proposal for updated UPW specifications
    • Update of potential solutions for WECC, AMC
    • Start work on new specifications for RH (metal exposure and reticle environment)
    • Proposal for acid definition updates
• **Recent activities:**
  
  - Discussion with assembly and packaging group to study yield modeling for typical back end process steps
  - YE WG looking for candidates to work on yield modeling activities

• **Ongoing:**
  
  - Bonding and debonding processes are the most important steps for yield in assembly and packaging
  - TSV yield issues to be discussed further
WECC: Ultra Pure Water

• **Recent activities:**
  – Bacteria and resistivity removed from YE3 table
  – Benchmarking study in US
  – Decision not to change the metal specifications for UPW
  – Proposal to split TOC into critical and non critical organics. Ongoing discussions on relevancy of specification levels.

• **Ongoing / planned activities:**
  – Better understanding of UPW organics and their control
  – Improve particle deposition models. Discuss relevancy of number and size of killer particles.
WECC: AMC

• Recent activities:
  – Introduction of AMC definition table
  – Update of potential solutions for 450 mm and reticle

• Ongoing / planned activities:
  – Introduction of moisture as new chemical contamination for critical processes and 193 nm / EUV reticle environments
  – Review potential contamination control challenges in NGL (e.g. EUV, nano-imprint and direct self assembly)
  – Investigate HNO$_2$ impact on different process steps and clarification of analytical procedures
  – Addition of a contamination control table for back end processes.
  – Review requirements for 450 mm manufacturing
Update on CIA/DDC activities

ITGW activity with Assembly & Packaging

Start Yield Enhancement discussion and strategy for assembly lines

Activities:

- set up a questionnaire
- include ongoing feedback from A&P

future
- finalize questionnaire based on input
- send out and collect input/comments
- summarize and analyze input
Update on CIA/DDC activities

ITGW activity with Factory Integration

Factory Integration is adding subchapter topics:
big data, control systems, prediction

-Subchapters on topics touching Yield Enhancement will be created in cooperation with YE-TWG

Status:
- Next steps will be defined in ITRS summer meeting and subsequently executed
Proposal of Japan concerning extension of CIA focus

• What to do?
  – Establish a better balance of defect/contamination detection and fault diagnostics / control of electrical characteristics in CIA focus
  – Include statistical / systematic approach into YE activities
  – Include device / chip / system level tables and requirements into ITRS YE chapter

• Why?
  Extra / Missing materials are root cause of yield excursion
  → Physical inspection often requires intensive efforts
  → Such faults are more easily approached by detection of abnormal device behavior / chip malfunction manifesting itself in out-of-spec electrical parameters
Proposed example of classification for CIA methodologies

Organizational approach is essential for efficient yield enhancement

<table>
<thead>
<tr>
<th>Root Cause Candidates</th>
<th>Time to capture defect</th>
<th>Isolation For PFA*1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSTEM</td>
<td>---/Yield Management System</td>
<td>Difficult</td>
</tr>
<tr>
<td>CHIP</td>
<td>--- /Diag. system</td>
<td>Very Difficult</td>
</tr>
<tr>
<td>CHIP</td>
<td>uSec /Logic Tester</td>
<td></td>
</tr>
<tr>
<td>DEVICE</td>
<td>mSec /Parameter Analyzer</td>
<td>Slightly Difficult</td>
</tr>
<tr>
<td>PROCESS</td>
<td>Sec /CD-SEM</td>
<td>Easy</td>
</tr>
</tbody>
</table>

Current focus of CIA chapter: physical defect detection on wafer (including particle / contamination)
Shrink of devices → lack of accordant measurement capacity

Objective of CIA: Identification of critical extra / missing materials based on integration of physical, electrical, functional or statistical observation
Proposed example of classification for CIA methodologies

Organizational approach is essential for efficient yield enhancement

<table>
<thead>
<tr>
<th>Time to capture defect</th>
<th>Isolation For PFA*1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Root Cause Candidates</td>
<td></td>
</tr>
<tr>
<td>---/Yield Management System</td>
<td>Difficult</td>
</tr>
<tr>
<td>Chip Fault Isolation</td>
<td></td>
</tr>
<tr>
<td>--- /Diag.system</td>
<td>Very Difficult</td>
</tr>
<tr>
<td>uSec /Logic Tester</td>
<td></td>
</tr>
<tr>
<td>Device Defect</td>
<td></td>
</tr>
<tr>
<td>mSec /Parameter Analyzer</td>
<td>Slightly Difficult</td>
</tr>
<tr>
<td>Process Defect</td>
<td></td>
</tr>
<tr>
<td>Sec /CD-SEM</td>
<td>Easy</td>
</tr>
</tbody>
</table>

Objective of CIA: Identification of critical extra / missing materials based on integration of physical, electrical, functional or statistical observation

Acquisition of electrical characteristics of devices in general faster than acquisition of values of the physical layer

*1 PFA: Physical Failure Analysis for root cause confirmation
Proposed example of classification for CIA methodologies

Organizational approach is essential for efficient yield enhancement

<table>
<thead>
<tr>
<th>Time to capture defect</th>
<th>Isolation For PFA*1</th>
</tr>
</thead>
<tbody>
<tr>
<td>---/Yield Management System</td>
<td>Difficult</td>
</tr>
<tr>
<td>--- /Diag.system uSec /Logic Tester</td>
<td>Very Difficult</td>
</tr>
<tr>
<td>mSec /Parameter Analyzer</td>
<td>Slightly Difficult</td>
</tr>
<tr>
<td>Sec /CD-SEM</td>
<td>Easy</td>
</tr>
</tbody>
</table>

Characteristics of chip layer:
Pass / Fail
Short test time for one pattern (compared to measurement of electrical characteristics), Fault diagnosis recognizes device defect

Objective of CIA: Identification of critical extra / missing materials based on integration of physical, electrical, functional or statistical observation
Proposed example of classification for CIA methodologies

Organizational approach is essential for efficient yield enhancement

- Time to capture defect
- Isolation for PFA*1
  - /Yield Management System: Difficult
  - /Diag.system: Very Difficult
  - uSec /Logic Tester
  - mSec /Parameter Analyzer: Slightly Difficult
  - Sec /CD-SEM: Easy

*1 PFA: Physical Failure Analysis for root cause confirmation

Objective of CIA: Identification of critical extra / missing materials based on integration of physical, electrical, functional or statistical observation
Outlook

Development / Improvement of the Yield Enhancement chapter

Discussion of the focus of YE chapter

- What are the pros and cons of referring to not only physical/process defects but also to device defects and abnormal electrical characteristics of a device?

- Does a change of emphasis in YE (CIA) activities make sense (e.g. with respect to the advent of MtM, inclusion of back end Yield, 450 mm technology)?

- What about including an improved combination of yield of products/fault diagnosis/control of electrical characteristics and defect/contamination detection of the wafer with the respective statistics in YE activities in order to achieve reasonable yield enhancement?

- Should we include tables for virtual metrology and for advanced control strategies?
Outlook

Development / Improvement of the YE chapter: Towards ITRS 2.0

- Reflection of current status and future requirements needs subsequent adjustment of outline and content of the chapter

- Keep tables for *Front End Processing* updated
- Add Back End Yield Enhancement specifications
- Look into *Assembly and Packaging* yield enhancement
- Intensify collaboration and align, see following slides, with
  - Factory Integration (WECC, AMC, UPW) short term
  - Metrology (DDC, CIA) short term
  - ESH (WECC) short term
  - Heterogenous Integration (YL) medium term
  - MtM (YL) medium term
  - Test & Design (for “Electrical Metrology”): No activity defined yet long term
Outlook ITRS 2.0: Definitions of 7 Focus Topics

**System Integration**—studies and recommends system architectures to meet the needs of the industry. It prescribes ways of assembling heterogeneous building blocks into coherent systems.

**Outside System Connectivity**—refers to physical and wireless technologies that connect different parts of systems.

**Heterogeneous Integration**—refers to the integration of separately manufactured technologies that in the aggregate provide enhanced functionality.

**Heterogeneous Components**—describes devices that do not necessarily scale according to “Moore's Law,” and provide additional functionalities, such as power generation and management, or sensing and actuating.

**Beyond CMOS**—describes devices, focused on new physical states, which provide functional scaling substantially beyond CMOS, such as spin-based devices, ferromagnetic logic, and atomic switch.

**More Moore**—refers to the continued shrinking of horizontal and vertical physical feature sizes to reduce cost and improve performance.

**Manufacturing** consists of tools and processes necessary to produce items at affordable cost in high volume.
### Outlook ITRS 2.0: Cooperation with 7 Focus Topics

<table>
<thead>
<tr>
<th>ITWG</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Integration (SI)</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outside SC (OSC)</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hetero Integration (HI)</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hetero Components (HC)</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>More Moore (MM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>More than Moore (MTM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>Factory Integration (FI)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>ERM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FEP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Litho</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>EHS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>Metro</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M&amp;S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Key**:
- X: Focus on this topic

---

**ITRS**

International Technology Roadmap for Semiconductors

Grenoble, October 7, 2014
www.iisb.fraunhofer.de