Hybrid Wafer Level Bonding for 3D IC
An Equipment Perspective
Markus Wimberger, Corporate Technology Development & IP Director
History & Roadmap - BSI CIS Devices

2009
Conventional BSI CIS – No 3D IC

2013
1st Generation 3D BSI CIS with vias at chip edge

????
2nd Generation 3D BSI CIS with connections in bonding interface

Source: EVG
BSI CIS Generation vs. Alignment Accuracy Requirements

<table>
<thead>
<tr>
<th></th>
<th>Interconnect Pitch</th>
<th>Global Alignment Accuracy</th>
<th>Distortion &amp; Runout</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>N/A 6 µm 3 µm (?)</td>
<td>&lt; 5 µm &lt; 0.5 µm &lt; 0.2 µm</td>
<td>Local (Distortion)</td>
</tr>
<tr>
<td>Gen II 3D BSI CIS</td>
<td></td>
<td></td>
<td>Global (Distortion &amp; Runout)</td>
</tr>
<tr>
<td>Gen I 3D BSI CIS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BSI CIS</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- With both wafers structured and high pitch interconnect designs, global alignment accuracy requirements are getting more tight.
- In order to ensure local alignment accuracy at every single point on the wafer, distortion and runout control are getting very important.

Source: EVG
Example: Sony ISX014

Source: http://techon.nikkeibp.co.jp/english/NEWS_EN/20130222/267487/

Source: Chipworks
CMOS Wafer Preparation for Oxide Bonding

Process flow: CVD oxide preparation for wafer bonding

Source: EVG
Plasma Activated Bonding

**Ex-situ Process Flow**

- Consecutive activation

**Initial Wafer Pair**

**Cleaning (optional)**

- EVG®300

**Activation**

- EVG®810LT

**Bonded Wafer Pair**

**Low Temperature Annealing**

- EVG®500

**Optical Alignment (optional)**

- SmartView® NT

Source: EVG
Bond Strength PAWB – vs. Annealing Temperature


Source: EVG
**Hybrid Bonding – Definitions, Principle**

**Definition:**

*Hybrid bonds are bonds that rely upon the formation of...*  

- **Metal Bond**
- **Dielectric Bond**

...at the same time

**Motivation & technical options**

- Metal shall provide electrical connection between two substrates
- Different elemental metals and eutectics may be use. Examples are:  
  - Cu-Cu  
  - Ni-Ni  
  - SnAgCu or AuSn Eutectic

- Dielectric shall provide additional mechanical strength to the interface and shall seal around metal pads to maintain isolation and to prevent metal corrosion. Frequently metal area is only <10% of total substrate surface.
- Two main options may be used:  
  - SiO$_2$ and / or SiN  
  - Organic Dielectrics
Hybrid Wafer Bonding – Examples & Advantages

The insulator material:
- Increases the bonding area to (close to) 100%
- Ensures electrical isolation between metal pillars

Ziptronix Direct Bond Interconnect (DBI™), Courtesy of Ziptronix

Metal/Adhesive Via First 3D Bonding; Courtesy of RPI
Adhesive (e.g. BCB):
+ Simple surface preparation
+ High yield process
- Thermal Bond → Alignment & Distortion? (has been solved)
- Cycle time for bonding process (30 to 60min)
- Front-end compatibility?
- Resistance against thermal processing (O2 free!)
- Process integration (via etching, etc.)

SiO2:
+ Front-end compatible
+ No organic materials
+ Process integration (etching)
+ Highly clean process
+ Very fast (~15 pairs per hour)
+ Better perspective to optimize distortion and alignment accuracy.
- More challenging surface preparation
Cu-Cu Bonding - Development Target

Bonding Process Conditions

Established bonding conditions

Target

Entire Process
Cu-Cu: Successful bonding @ 175° C

The key for low temperature Cu Bonding is a reliable oxide removal process

Source: EVG
Successful Wafer Bonding Requirements

- **Global Wafer Shape**
  - Flatness, Total Thickness Variation (TTV)
  - Bow/Warpage

- **Substrate Surface Quality**
  - Smoothness
  - Microroughness < 0.5nm rms

- **Cleanliness**
  - Particles
  - Organic residuals
  - Metal ions

 Incoming Materials Specification

- **Cleanliness**
  - Particles
  - Metal ions

- **Proper Surface Activation**
  - Surface-to-surface contact procedure

Control assisted by EV Group Tooling
Hybrid Bonding - General Considerations

Since Metal and dielectric are bonded at the same time, material and process conditions have to be optimized and guaranteed for both metal and dielectric regions on the wafer at the same time as well.

Key considerations for Metal TC bond

- Surface flatness and roughness
- Free of particles
- Oxide management
- Metal cleanliness

Key considerations for SiO$_2$ or SiN bond

- Surface flatness and roughness
- Free of particles
- Surface preparation to achieve high bonding strength at low annealing temperature

Selected preparation and / or cleaning processes have to be compatible with Metal and SiO2 / SiN surfaces
Hybrid Bonding – Working Principle

Surface preparation for both surfaces for:
- Cleanliness (final particle removal)
- Metal oxide removal
- Activation of SiO₂ or SiN surface for development of high bonding strength

Typically wet cleaning and plasma activation are employed for surface preparation. Wet cleaning may include the use of chemicals for metal oxide removal.
Hybrid Bonding – Working Principle

Process Flow

Surface Cleaning

Surface Activation

Pre-Bonding

Temperature Profile

Prebonding of wafers

- Wafers will be aligned using F2F precision optical alignment. This will enable sub-μm alignment precision.
- Once aligned, wafers will be put in contact at room temperature and in regular cleanroom atmosphere.
- Optimized tooling and process sequences will ensure that sub-μm alignment precision is maintained across the entire wafer.
Hybrid Bonding – Working Principle

Dielectric Bond Annealing

- The first stage of the thermal annealing process is designed to strengthen the bond between the dielectric surfaces while minimizing the stress in the interface due to differences in CTE between metal and dielectric materials.
- Dielectric bonds can be annealed at temperatures as low as 100 to 150°C.
**Hybrid Bonding – Working Principle**

**Process Flow**
- Surface Cleaning
- Surface Activation
- Pre-Bonding
- Dielectric Bond Annealing
- Metal Bond Annealing

**Temperature Profile**

**Metal Bond Annealing**
- Heating the bonded pair to higher temperatures will result in pressure being built up at the metal pad surfaces thanks to the higher CTE of metal as compared to SiO$_2$ or SiN.
- The increased temperature and the pressure will result in metal diffusion at the interface of the metal pads and grain growth across the bond interface.
Hybrid Bonding – Working Principle

Process Flow:
- Surface Cleaning
- Surface Activation
- Pre-Bonding
- Dielectric Bond Annealing
- Metal Bond Annealing

Temperature Profile:

Completed bond:
- The described process sequence will result in the formation of strong bonds for both metal and dielectric surfaces at the same time.

Ziptronix Direct Bond Interconnect (DBI™), Courtesy of Ziptronix
Materials Flow – Bonding and Inspection

Bonding – Gemini FB

Inspection

Alignment – EVG40NT
C-SAM

Data Feed Forward

Patent Pending
SmartView® Face-to-Face Bond Aligner

- Proprietary Alignment Technique that allows for high alignment accuracy as needed for high density interconnects with **non-IR transparent wafers**.

  - **No Z-travel**
    - Locate bottom wafer alignment marks with top objectives
    - Digitize image
    - Store position

  - **No re-focussing**
    - Align top wafer to digitized image

  - **Perfect result**
    - Restore bottom wafer position
    - Bring wafers in contact

Source: EVG

US Patent: 6,214,692 B1
SmartView® NT Results

<200nm (3 Sigma) Alignment Capability
Overlay Alignment Data

Measured Data

> 0 nm
< 200 nm

> 200 nm
< 350 nm

> 350 nm
< 500 nm
Summary and Conclusions

• Novel 3D image sensor structures require more advanced bonding technologies that enable formation of electrical connections.

• Hybrid bonding offers promise as the technology of choice for high density 3D integration.

• Latest generation bonding equipment technology enables implementation of hybrid bonding technology in high volume manufacturing of devices with ultra-high-density interconnects.