“Packaging in Europe – Advances in System Integration on Wafer Level”

Steffen Kröhnert, Director of Technology, NANIUM S.A.
José Campos, Senior Manager R&D, NANIUM S.A.
More-than-Moore = Value Adding Packaging has Potential in Europe!

• Target: 20% of global semiconductor manufacturing back to Europe by 2020.
• Entire Supply Chain need to be considered, Packaging is an important part of it.
• Chip-Package-Board Co-Design and Co-Development essential for fast time-to-market and low cost.
• NANIUM, as largest Packaging Foundry in Europe:
  – More-than-Moore on 200mm and 300mm, Wafer Level System-in-Package (WLSiP) ✓
  – 450mm PreAssy/ DieBond, Fan-In WLP, Fan-Out WLP ?!
  – 450 x 450mm² Panel based Fan-Out WLP ?!
NANIUM was founded in February 2010.
We provide contract Assembly and Engineering Services for WLP, Packaging, Assembly & Test.
World-Class Facility @ West Coast of Europe
Largest Packaging Foundry/ OSAT in Europe

A state-of-the-art facility located in Vila do Conde, North of Porto, Portugal.

- 520 employees, thereof 140 Engineers
- 222,000 ft² clean room (20,600 m²)
- > $1B cumulated investment
- Current Capacity:
  - 4,000 wafer/ week – 300mm FI & FO
  - 2,000 kpcs/ week – BGA Components
  - 2,700 pcs/ week – SMT Modules

24/7 Operation
World-Class Facility @ West Coast of Europe

Largest Packaging Foundry/OSAT in Europe
NANIUM’s Four Business Offers
All Under one Roof: Wafer Processing to Board Assembly

1-High Volume Packaging, Assembly & Test Services
- Organic Laminate Based BGA Packages
- More Complex Packages Like MCM, MCP and SiP
- Leadframe Packages
- SMT Board Assembly

2-High Volume 300mm WLP & Wafer Test Services
- RDL Processing
- Fan-In WLP / WLCSP
- Fan-Out WLP / eWLB
- Wafer Test
- Wafer Thinning
- Wafer Molding
- Wafer Bumping

3-Flexible Pilot Line for Packaging, Test & SMT
- Fast Prototype and Qualification Runs
- Production of Small Series
- Innovative Fast Quality Package Prototypes
- Flexible Technology Diversity Management
- Technology Transfer

4-Turnkey Engineering Services R&D, Laboratories & Consulting
- Package Development
- Test Engineering & Development
- Quality & Supply Chain Management
- Advisory Services
- Laboratories
Value Adding Packaging / More-than-Moore
The Role of Packaging is Changing

The One Chip Problem – Custom IC costs continue to increase

- Increasing cost per tapeout drives down # tapeouts
- Increasing demand for another way to get custom hardware

Source: eSilicon 2012
Value Adding Packaging / More-than-Moore
The Role of Packaging is Changing

**System-on-Chip**

**Single Chip SOC**
Containing 1 SOC
(*assembled in Single Die Package*)

**System-in-Package**

**Multi Chip SIP**
Containing >1 SOC + other dies/ components
(*assembled in more complex Multi Die Package*)
Hybrid Package Assembly
Combination of Different Interconnect Technologies

- Wire Bonding
- RDL
- Bumping
- SMT
- Flip Chip or WLCSP
- Molding
- Globtop
- Dam & Fill
- Underfill
Value Adding Packaging / More-than-Moore Package Level → Wafer Level System Integration

- Consumer Market / Mobile Applications are main driver of advanced packaging technology development

- How to handle the critical triad of packaging: “Performance, Form Factor and Cost”?

- The two general directions for packaging:
  
  **Driver:** Cost, Performance, Miniaturization  
  **Solution:** Large Scale Panel, Batch Processing  
  → Wafer Level Packaging (WLCSP)  
  
  **Driver:** More functionality on same or less space  
  **Solution:** System Integration, „More than Moore“  
  → System-in-Package (SIP)
Value Adding Packaging / More-than-Moore
Package Level ➔ Wafer Level System Integration

• Today the majority of SiP is realized using laminated organic substrate based packages (BGA and LGA);
• Need to close the gap to System-on-Chip (SoC) performance, where short connections between the functional areas are inherent.
Value Adding Packaging / More-than-Moore
Wafer Level System Integration

WLSiP
by eWLB
WLSiP enabled by eWLB
Wafer Level System Integration

The eWLB*) FO-WLP technology is based on:

1) BE wafer on a carrier with KGD’s (reconstituted Backend wafer);
2) Wafer Level Compression Molding;

*) eWLB (embedded Wafer Level Ball Grid Array) is patented by Infineon Technologies AG
WLSiP enabled by eWLB

Wafer Level System Integration

3) RDL using Thin Film Technology;
4) Wafer Level Pre-formed Bump Drop Process (Solder Ball Attach);
5) Wafer Level Component Marking and Singulation Process.

- Based on Infineon/ Intel MCG-IMC eWLB technology
- First ever 300mm Fan-out WLP realization!
- Production line in high volume since Q3/2010
- Shipped more than 370 Million (E09/13) eWLB packages since!
- Proven technology with 99% plus yield levels

5x5m² chip in 8x8x0.8mm³ package
0.800mm package height w/ solderballs
183 solderballs 0.300mm initial dia
0.230mm ball height, 0.500mm pitch
WLSiP Developments based on eWLB
Very Small WLSiP

- System integration required for Consumer Market:
  - Increased functionality in less space – “More than Moore”
  - Lowest package dimension
  - Lowest cost

- SiP eWLB multi-die package:
  - Side-by-Side and Stacked C2W
  - Minimum die-to-package edge distance
  - Minimum die-to-die distance
  - Increased Si content (Si occupation rate)

- Example of application: Sensor & ASIC SiP (MEMS)
Example of Test Vehicle 1:

- Package size = 4.7mm²
- Package Height < 1.0mm
- Si ratio = 69%
- Nr. I/Os per package = 10
- Min. die-to-package edge distance = 100µm
- Die-to-die distance < 200µm
- Multi-Design reconstituted wafer
- Nr. systems per 300mm reconstituted wafer > 13,000
WLSiP Developments based on eWLB
Very Small Side-by-Side WLSiP

- Example of a reconstituted 300mm wafer

Wafer Reconstitution
Chip Carrier

Reconstituted Wafer after Molding

Later Final Package (WLSiP)
WLSiP Developments based on eWLB
Very Small Side-by-Side WLSiP

- Example of Test Vehicle 2:
  - Module size = 3mm²
  - Die Thickness = 150um
  - Nr. dies per module = 3
  - Min. die size = 250um
  - Min. die-to-pkg edge distance = 250um
  - Die-to-die distance = 380um
  - Nr. systems per 300mm reconstituted wafer > 50,000

Proprietary information not disclosed
WLSiP Developments based on eWLB
Very Small Side-by-Side WLSiP

- Example of a reconstituted 300mm wafer

Proprietary information not disclosed

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WLSiP Developments based on eWLB
Small Stacked C2W WLSiP („Hanging Die“)

- **Example of Test Vehicle:**
  - Package size = 16mm²
  - Package Height < 0.8mm
  - Flip-Chip Assy on eWLB Wafer
  - Reduced Chip-to-chip vertical interconnection
High Density Integration for Customer Applications:
- Enhanced electrical & thermal performance
- Substrate less technology
- Smaller form factor & reduced module thickness

SiP eWLB with Side-by-Side Multi-Die Package:
- Increased number of active dies (realized up to 10)
- Minimum die-to-die distance
- RDL & u-bumping & Edge Connectors as a replacement of interposers and other interconnect elements
WLSiP Developments based on eWLB
Highly Integrated Side-by-Side WLSiP

- **Example of Test Module:**
  - Module size = 920mm²
  - Module Height < 0.5mm
  - Nr. dies per module = 10
  - Die-to-die distance < 130um
  - Nr. I/Os per module > 6000
  - u-Bump height = 10um
  - Edge connectors

- **u-Bump Profile Scanning**

- **Edge Connectors**

- **u-Bumping Array**
WLSiP Developments based on eWLB
Heterogeneous Integration using FO-WLP

- **Heterogeneous Integration for Flexible Product Design:**
  - Easy integration of active & passive devices
  - Flexible integration of devices of different types and with different form factors
  - Multi-Design Reconstituted Wafer
  - Enabling of 3D Stacking

Wirefree Die-on-Die (WDoD™)
Wafer Level Stack - WDoD™ is Trademark of 3D Plus S.A.

WDoD is...
- Recon wafer using standard KGD (Known Good Die) without TSV;
- Wafer Level Stacking, laminated substrate free technology;
- Unique capability to stack several different dies and packages;
- Less weight and volume compared to the existing 3D solutions;
- Test and Burn-in capability for each layer prior to stacking.
WLSiP Developments based on eWLB
Heterogeneous Integration using FO-WLP

Heterogeneous 3D-SiP eWLB Multi-Die Package:

- Increased number of active & passive devices
- Minimum die-to-die distance
- Handling very small dies
- Multi Layer RDL and reduced via opening
- Handling different loading media and device thicknesses
- 3D Stacking enabling by using eWLB & WDoD™
WLSiP Developments based on eWLB
Heterogeneous Integration using FO-WLP

- Example of Test Module 1:
  - Module size ~ 38mm²
  - Module Height = 0.2mm
  - Nr. dies per module = 2 active + 7 Cap + 1 Diode
  - Die-to-die distance < 200um
  - Minimum die size = 660um
WLSiP Developments based on eWLB
Heterogeneous Integration using FO-WLP

- **Example of Test Module 2:**
  - Module size = 361mm²
  - Module Height = 0.2mm
  - Number of active dies per module = 3
  - Die pad size & pitch = 47um / 52um staggered
  - Multi Layer RDL
  - Via opening = 15um
  - Line Width/ Space = 20/20um
FO-WLP (eWLB) Technology Roadmap
Markets and Applications Enabling

**Legend:**
- Required R&D Time
- Available
- R&D Activities ongoing

**Customer Application**
- Wireless Consumer
- MEMS/ Sensors Consumer
- Radar / mmWave Automotive
- Fiber Optics / LED / Photonics
- Sensor/ ASIC Arrays
- Heterogeneous Integration, Medical & Security
- Mixed Signal ASIC, RF & High Power Dissipation
- Stacked DRAM / PoP
- MEMS/ Sensors Automotive

**Technology Platform Development**

**Source:** Infineon
FO-WLP (eWLB) Technology Roadmap

RDL (Redistribution Layer)/ Package Construction

Legend:
- **Required R&D Time**
- **Available**
- **R&D Activities ongoing**

- **NEW**
- **1L Cu + UBM (thick Cu)**
- **2L Cu (w/ PI)**
- **Ni/Au thick UBM (for LGA pkg)**
- **3L Cu**
- **1L Cu + UBM (w/ WPR)**
- **1L Cu (w/ PI)**
- **2L Cu (w/ WPR)**
- **1L Cu + UBM (Ni/Au)**
- **3L Cu**

- **FS + BS RDL, PoP w/ TPV**
- **Frontside (FS) RDL**
- **Available**

- **No. of Layers**
- **RDL / UBM**
- **RDL Sides**
- **PoP**
FO-WLP (eWLB) Technology Roadmap
WLSiP (System-in-Package on Wafer Level)

Passives Integration

Min. Die-to-Die Clearance (x,y)

Multichip Package / SiP

Legend:
Required R&D Time
Available
R&D Activities ongoing
Outlook – Ongoing Developments

Package Thickness Reduction

- Development of BGA Package $< 0.5\text{mm}$ using BSP configuration

- Development of LGA package $< 0.35\text{mm}$ using Overmold configuration
Outlook – Ongoing Developments

Package Thickness Reduction

- Development of BGA Package $< 0.4\text{mm}$ using Overmold configuration for PoP bottom package
- Total package height of full PoP $< 1.0\text{mm}$
eWLB is a FO-WLP technology that presents competitive advantages to enable SiP solutions on Wafer Level.

NANIUM successfully completed several development projects on its FO-WLP eWLB technology for WLSiP.

NANIUM developed successfully several WLSiP test vehicles & demonstrators for its customers, e.g.:

- Very small SbS WLSiP,
- Small Stacked C2W WLSiP,
- Highly Integrated SbS WLSiP,
- Heterogeneous Integration WLSiP.

These developments extend the capabilities of FO-WLP eWLB and enlarge application fields for SiP solutions.
Questions?

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Silicon Saxony Pavilion