“More Package, Less Board - System Integration on Component and Wafer Level for More Performance on Less Space”

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More-than-Moore = Value Adding Packaging has Potential in Europe!

- Target: 20% of global semiconductor manufacturing back to Europe by 2020.
- Entire Supply Chain need to be considered, Packaging is an important part of it.
- Chip-Package-Board Co-Design and Co-Development essential for fast time-to-market and low cost.
- NANIUM, as largest Packaging Foundry in Europe:
  - More-than-Moore on 200mm and 300mm, Wafer Level System-in-Package (WLSiP)
  - 450mm PreAssy/ DieBond, Fan-In WLP, Fan-Out WLP
  - 450 x 450mm² Panel based Fan-Out WLP
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- 1.2 Technical Capabilities and Business Offers

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- 2.4 System-in-Package on Component Level (SiP) and Wafer Level (WLSiP)

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- 3.2 E2: System-in-Package, Organic Laminated Substrate Based (SiP)
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4. Summary and Conclusions
NANIUM was founded in February 2010.

We provide contract Assembly and Engineering Services for WLP, Packaging, Assembly & Test.
World-Class Facility @ West Coast of Europe
Largest Packaging Foundry/ OSAT in Europe

A state-of-the-art facility located in Vila do Conde, North of Porto, Portugal.

- 520 employees, thereof 140 Engineers
- 222,000 ft² clean room (20,600 m²)
- > $1B cumulated investment
- Current Capacity:
  - 4,000 wafer/ week – 300mm FI & FO
  - 2,000 kpcs/ week – BGA Components
  - 2,700 pcs/ week – SMT Modules

24/7 Operation
World-Class Facility @ West Coast of Europe
Largest Packaging Foundry/ OSAT in Europe
NANIUM’s Four Business Offers
All Under one Roof: Wafer Processing to Board Assembly

1- High Volume Packaging, Assembly & Test Services
- Organic Laminate Based BGA Packages
- More Complex Packages Like MCM, MCP and SiP
- Leadframe Packages
- SMT Board Assembly

2- High Volume 300mm WLP & Wafer Test Services
- RDL Processing
- Fan-In WLP / WLCSP
- Fan-Out WLP / eWLB
- Wafer Test
- Wafer Thinning
- Wafer Molding
- Wafer Bumping

3- Flexible Pilot Line for Packaging, Test & SMT
- Fast Prototype and Qualification Runs
- Production of Small Series
- Innovative Fast Quality Package Prototypes
- Flexible Technology Diversity Management
- Technology Transfer

4- Turnkey Engineering Services R&D, Laboratories & Consulting
- Package Development
- Test Engineering & Development
- Quality & Supply Chain Management
- Advisory Services
- Laboratories
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4. Summary and Conclusions
Functionality Integration
More Package, Less Board

Smart Phone Assembly
(Driver for Technology and Volume)

**Yesterday**
- Sony-Ericsson
  - Xperia – X10
- PCB area to Phone area ≈ 90%
- P+M+C area to total phone area ≈ 18%

**Today**
- Apple
  - iPhone 5
- PCB area to Phone area ≈ 30%
- P+M+C area to total phone area ≈ 9%

- Wirebond
- BGA/ LGA Packages
- FlipChip BGA,
  - Stacked MCP
  - PoP

Source:
*Phil Marcoux, PPM Associates 2012*
Functionality Integration
More Package, Less Board

• „The Board is Moving Inside the Package“
  • Embedded passives and actives
  • Side-by-Side goes 3D assembly in package (stacking) & PoP
  • 2.5D Si/ Glass interposer reduce the need for organic HDI PCB

• „SMT is Moving Inside the Package“
  • Wirebond goes FC, micro-solder bumps and copper pillars
  • Discrete passives move closer to active die inside the package
  • System-in-Package, reduced number of packages
Functionality Integration
More Package, Less Board

• More Package ≠ More Packages, but larger, more complex packages
• Increasing Integration Density
• Less Standard, More Customized

• **Overall System Optimization**
  • Performance towards SoC
  • System Miniaturization
  • System Cost Reduction

• Enhance product differentiation with features not available in standard solutions
• Improved Reliability due to Less Components and Less Interconnects

"More Package“
= More Performance

"Less Board“
= Less Space

Source:
ON-Semiconductor 2013
Functionality Integration
More Package, Less Board

• Trend driven by
  • Performance needs
  • Form Factor needs
  • System Cost reduction

• Trend with „Winners“ and „Losers“ along the Supply and Value Chain

• Need is understood, but ecosystem is not yet ready for the change
  • Organizational Setup
  • System Thinking
  • Consequent Co-Design
  • Customer is the winner

Source: ON-Semiconductor 2013
Value Adding Packaging / More-than-Moore
The Role of Packaging is Changing

- Assembly & Packaging was simply needed to:
  - Protect the chip;
  - Get it into the tester;
  - Get it mounted to the board w/ available SMT;
  - Redistribution of the contacts due to the pitch gap die-to-board.

- System integration on package level adds value to the product:
  - SIP and finally SOP as complimentary, but also alternative integration technology compared to SOC.
Value Adding Packaging / More-than-Moore

The Role of Packaging is Changing
Value Adding Packaging / More-than-Moore

SOC and SIP will Coexist

- System-on-Chip (SOC) = “More Moore”
  - The effect of CMOS miniaturization
  - … and the increasing importance of power/heat dissipation

![Image showing node progression and power dissipations](image)

Source: ITRS Roadmap 2008
Value Adding Packaging / More-than-Moore
SOC and SIP will Coexist

e.g.
Cypress PSoC Technology Platform

PSoC = Programmable System-on-Chip

System-on-Chip is from **performance** and from **formfactor** point of view always the best solution

- Cost ?
- Time-to-Market ?
- Flexibility ?

Source: Cypress Semiconductor 2013
Value Adding Packaging / More-than-Moore
SOC and SIP will Coexist

In this communication product, PSoC technology reduced the BOM from 12 ICs to 3 ICs by integrating FSK detector, voltage monitoring, DTMF and ringtone generation.

With the PSoC Technology Platform you can:

Source: Cypress Semiconductor 2013
Value Adding Packaging / More-than-Moore

The Role of Packaging is Changing

The One Chip Problem – Custom IC costs continue to increase

- Increasing cost per tapeout drives down # tapeouts
- Increasing demand for another way to get custom hardware

Source: eSilicon 2012
Value Adding Packaging / More-than-Moore

The Role of Packaging is Changing

- **Single Chip SOC**
  - Containing 1 SOC
  - (assembled in Single Die Package)

- **Multi Chip SIP**
  - Containing >1 SOC + other dies/components
  - (assembled in more complex Multi Die Package)
Hybrid Package Assembly
Combination of Different Interconnect Technologies
Value Adding Packaging / More-than-Moore Package Level System Integration

- Why 3D and 2.5D Interposer compared to Organic HDI PCB?
  - Shorter interconnects between dies, less noise, more speed
  - Higher density, smaller footprint / Adoption to BGA pitch for PCB

Source: Phil Marcoux, PPM Associates 2012
Value Adding Packaging / More-than-Moore Package Level System Integration

- Why 3D and 2.5D Interposer compared to Organic HDI PCB?
  - RELIABILITY - The advantage of the “Reliability Pyramid”

Source: Phil Marcoux, PPM Associates 2012
Value Adding Packaging / More-than-Moore
Package Level ➔ Wafer Level System Integration

- Consumer Market / Mobile Applications are main driver of advanced packaging technology development

- How to handle the critical triad of packaging: “Performance, Form Factor and Cost”?

- The two general directions for packaging:

  | Driver: Cost, Performance, Miniaturization | Solution: Large Scale Panel, Batch Processing |
  | ➔ Wafer Level Packaging (WLCSP) |

  | Driver: More functionality on same or less space |
  | Solution: System Integration, „More than Moore“ |
  | ➔ System-in-Package (SIP) |
Value Adding Packaging / More-than-Moore

Package Level → Wafer Level System Integration

- Today the majority of SiP is realized using laminated organic substrate based packages (BGA and LGA);
- Need to close the gap to System-on-Chip (SoC) performance, where short connections between the functional areas are inherent.
Value Adding Packaging / More-than-Moore
Wafer Level System Integration

WLSiP
by eWLB
WLSiP enabled by eWLB
Wafer Level System Integration

The eWLB*) FO-WLP technology is based on:

1) BE wafer on a carrier with KGD’s (reconstituted Backend wafer);
2) Wafer Level Compression Molding;

*) eWLB (embedded Wafer Level Ball Grid Array) is patented by Infineon Technologies AG
WLSiP enabled by eWLB
Wafer Level System Integration

The eWLB FO-WLP technology is based on:

3) RDL using Thin Film Technology;
4) Wafer Level Pre-formed Bump Drop Process (Solder Ball Attach);
5) Wafer Level Component Marking and Singulation Process.

5x5m² chip in 8x8x0.8mm³ package
0.800mm package height w/ solder balls
183 solder spheres 0.300mm
0.230mm ball height, 0.500mm pitch,
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| 4. Summary and Conclusions |
E1: Multi Chip Package
Organic Laminated Substrate Based

Dual-Face-Down Multichip Package

- xFD™ Technology is Trademark of Invensas Corporation

DFD is ...
- Denser: At least 30% thinner than conventional MCP;
- Faster: Due to ultra-short and separated interconnects;
- Cheaper: Single die level performance in a multichip package;
- Lower material cost (no RDL needed, shorter Au wire);
- Using standard BGA assembly manufacturing line.

Available

- 2012: DFD w/ 1Gb DDR3
- 2013: DFD low profile w/ 1Gb DDR3, DFD w/ 2Gb DDR3, DFD w/ 1Gb DDR3
- 2014: QFD w/ 1Gb DDR3
E1: Multi Chip Package
Organic Laminated Substrate Based

Single Die Package ("SDP")
60 – 96 ball configurations
(Tessera invention used by DDR2/DDR3)

Dual Face Down ("DFD")
104 – 112 ball configurations

Quad Face Down ("QFD")
243 ball configuration

Source: Invensas Corp 2012
E1: Multi Chip Package
Organic Laminated Substrate Based

**Component maker benefits:**
- Lowest cost way to assemble DRAM die
  - Cost/DRAM die assembled is lower than other methods including single die
- Test yields better than other DDPs
  - Symmetric performance of both die in package

**System OEM benefits:**
- Avoids need for costly HDI PCBs for system use
  - Design studies show non-HDI PCBs viable for thin form-factor clients when using xFD
- Reduces memory system footprint on PCB
  - Design studies show smaller PCB footprints for solder-down memory application in thin form-factor clients
  - Allows larger components on PCB for non-HDI deployment

Source: Invensas Corp 2012
E1: Multi Chip Package
Organic Laminated Substrate Based

Dual Inline Memory Module (DIMM) Solder-down on System Board

Original Design (3-6-3 HDI PCB)

Source: Invensas Corp 2012
E1: Multi Chip Package
Organic Laminated Substrate Based

Invensas DFD:
Dual Channel Single Rank (non-HDI PCB)
E1: Multi Chip Package
Organic Laminated Substrate Based

Invensas QFD:
Dual Channel Dual Rank
(non-HDI vs. HDI PCB)

Quad Die DRAM Packages:
Quad 16 bit organization, Top and Bottom Placement on PCB

Source:
Invensas Corp 2012
E1: Multi Chip Package
Organic Laminated Substrate Based

- Reference Platform used 3-6-3 HDI PCB technology
  - Cost is $X$
  - *HDI PCB prototyping takes $Y$ weeks*

- Non-HDI, plated through hole via 12 layer PCB achievable using DFD/QFD
  - Cost is $\frac{1}{4}X$
  - *12 layer non-HDI PCB prototyping takes $\frac{1}{4}$ the time for HDI*

*Lower cost, lower schedule risk using non-HDI PCB*

Source:
Invensas Corp 2012
E2: System-in-Package
Organic Laminated Substrate Based

- Set Top Box for Digital TV SiP 27x27mm²

Typ A – BGA Package
E2: System-in-Package
Organic Laminated Substrate Based

Controller die – (1x) flip-chip:
Die size: 8.0x8.3mm², Number of bumps: 900

Package Size: 27x27mm²

Memory dies – (2x) face-up w/ wire bond:
2x 2G DDR2 (x16 org), Die size: 5.5x7.6mm²
E2: System-in-Package
Organic Laminated Substrate Based

Flash die - (1x) face-up wire bond: Die size: 6.4x 8.3mm²
0201 SMD Passives - (23x) Component size: 0.6x0.3mm²

Dimensional Design Characteristics:
- HDI PCB technology type II
- Trace-to-trace pitch 36µm (required under FlipChip)
- Route technology 18/18µm (15/15µm available in volume)
- Via Drill/Lands 60µm/120µm
- 4 Layers substrate with total thickness 1.0mm (2 signal + 2 plan layers)
- Final component thickness with solder balls 2.5mm
E2: System-in-Package
Organic Laminated Substrate Based

- Set Top Box for Digital TV non-SiP
  Required Board Space 50x60 mm²

Dimensional Design characteristics:
- Trace-to-trace pitch 150µm
- Route technology 75/75µm
- Via Drill/Lands 150µm/300µm
- 2 Layers substrate

BGA Pkg Controller (Flip-Chip):
- Size: 27x27mm²
- Die size: 8.0x8.3mm²
- Number of Solder Balls: ~600
- Ball Pitch: 1000µm

BGA Flash Package:
- Size: 8x10mm²
- Die size: 6.4x 8.3mm²
- Number of Solder Balls: 64
- Ball Pitch: 800µm

BGA Memory Package:
- Size: 8x12.5mm²
- Die Size: 7.6x9.2mm²
- Die size:5.5x7.6mm²
- Number of Solder Balls: 84
- Ball Pitch: 800µm
E2: System-in-Package
Organic Laminated Substrate Based

- Set Top Box for Digital TV **SiP** 27x27mm²
- Set Top Box for Digital TV **non-SiP** Required Board Space 50x60 mm²

Form Factor = \( \frac{27 \times 27}{50 \times 60} = 24.3\% \)
> 4x area would be needed for non-SiP
E3: System-in-Package
Wafer Level Based / eWLB Technology (WLSiP)

- Medical Application WLSiP (eWLB) 5.2x7.3 mm²

Die U5 – Recon, RDL, Die size: 3.2x3.2mm²
Number of pads to be connected: 56

Die U1 – Recon, RDL, Die size: 3.8x1.6mm²
Number of pads to be connected: 33

PICS (Passive Integrated Connecting Substrate)
- (7x) Component size: 1.160x0.660mm²

Die U6 – Recon, RDL, Die size: 1.5x0.5mm²
Number of pads to be connected: 6

Dimensional Design Characteristics:
- 56 Connected balls
- LGA landing pad pitch 0.5mm
- Trace-to-trace pitch 40µm
- Route technology 20/20µm
- Via Opening 20µm
- 1 RDL (total 25µm w/ Dielectric layers)
- Final component thickness 0.200mm
E3: System-in-Package
Wafer Level Based / eWLB Technology (WLSiP)

- Medical Application non-WLSiP (eWLB)
  Required Board Space 8x10.5 mm²

U5 - BGA FO WLP (eWLB):
- Size: 5.0x5.5mm²
- Die size: 3.2x3.2mm²
- Number of Solder Balls: 56
  (Matrix: 7x8 balls)
- Ball Pitch: 500µm

U1 - BGA FO WLP (eWLB):
- Size: 4.5x3.0mm²
- Die size: 3.8x1.6mm²
- Number of Solder Balls: 36
  (Matrix: 8x5 balls)
- Ball Pitch: 500µm

U6 – BGA FO WLP (eWLB):
- Size: 2.0x1.5mm²
- Die Size: 1.5x0.5mm²
- Nr. of Solder Pads: 6
  (Matrix: 2x3)
- Ball Pitch: 500µm

Dimensional Design Characteristics:
- Trace-to-trace pitch 150µm
- Route technology 75/75µm
- Via Drill/Lands 150µm/300µm
- 1 Layer PCB

PICS ➔ 0201 SMD Passives
**E3: System-in-Package**

Wafer Level Based / eWLB Technology (WLSiP)

- Medical Application **WLSiP** (eWLB) 5.2x7.3 mm²
- Medical Application **non-WLSiP** Required Board Space 8x10.5 mm²

Form Factor = \( \frac{5.2 \times 7.3}{8 \times 10.5} = 45.2\% \)

> 2x area would be needed for non-WLSiP
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4. Summary and Conclusions
Summary & Conclusions

- The role of Packaging is changing significantly
- Value adding Packaging by integration of product functionality
- Performance, foot print and system cost are main drivers
- Single Chip SoC moves to Multi Chip SiP
- SoC in single die package and SiP in multi die package will coexist
- Many SiP will have one or even more SoC inside
- „The Board is Moving Inside the Package“
- „SMT is moving inside the Package“
- 3 Product Examples have been shown: 2x-4x Reduction of required board space was achieved by usage of SiP / WLSiP
- More Package, Less Board for More Performance at Less Space
- The whole System has to be considered, Co-Design is essential
Questions?

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