System-in-Package (SiP) on Wafer Level, Enabled by Fan-Out WLP (eWLB)

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Outline

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● Introduction to FO-WLP eWLB/ WLSiP
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Short Company Overview NANIUM

- NANIUM was founded in February 2010.
- We offer Packaging, Assembly and Test (OSAT).
- Design, Development, Engineering & Manufacturing.
Short Company Overview NANIUM

- State-of-the-Art facility located in Porto, Portugal.
- 520 Employees, thereof 140 Engineers (July 2012).
- 222,000 ft² (20.600 m²) Clean Room (1K, 10K, 100K).
- Cumulated Investment $1B.
Short Company Overview NANIUM

- Package Design & Development
- Test Engineering & Development
- Quality & Supply Chain Management
- Reliability, Failure Analysis Labs
- Advisory Services

- Fan-In WLP
- Fan-Out WLP (eWLB)
- Wafer Bumping (RDL, UBM)
- Wafer Test
- Wafer Thinning & Dicing
- Wafer Molding

- Fast Prototypes and Qualification Runs
- Production of Small Series
- Innovative Package Solutions
- Flexible Technology Diversity
- Technology Transfer

- Laminated Organic Substrate Based Packages (BGA/LGA)
- Complex MCP, MCM & SIP
- Stacked Die Packages
- Performance Optimized Solutions
- MEMS & Sensor Packaging

www.nanium.com
Introduction to FO-WLP eWLB/ WLSiP

- FO-WLP technology eWLB (embedded Wafer Level Ball Grid Array) introduced by Infineon Technologies AG;
- Creation of „Backend Wafer“ by wafer RECONSTITUTION with KGD, components, ... (pick & place, overmolding);
- Thin film REDISTRIBUTION layers, bumping and singulation.
Introduction to FO-WLP eWLB/ WLSiP

200 Mio eWLB Components Shipped

Semiconductor Packaging, Assembly and Test

High Volume Manufacturing in Europe

October 2010 – October 2012
Value Adding Packaging

- Assembly & Packaging was simply needed to:
  - Protect the chip;
  - Get it into the tester;
  - Get it mounted to the board w/ available SMT;
  - Redistribution of the contacts due to the pitch gap die to board.

- System integration on package level adds value to the product:
  - SiP and finally SOP as complimentary, but also alternative integration technology compared SOC.
Value Adding Packaging

- **MCM, MCP, SiP Definition**

  - **MCM**
    - 2D / planar
    - same dies

  - **MCP**
    - 2D+3D / stacked
    - different dies

  - **SiP**
    - 2D / planar / passives
    - autonomous system
    - "MCP-SiP"

  - **SiP**
    - 2D+3D / passives
    - autonomous system
    - "MCM-SiP"

  Source: ALTOS
Value Adding Packaging

- Today the majority of SiP is realized using laminated organic substrate based packages (BGA and LGA);
- Need to close the gap to System-on-Chip (SoC) performance, where short connections between the functional areas are inherent;
- HVM batch processing;
- Substrate-less, lower cost.
Value Adding Packaging

● How to handle the critical triad of packaging: “Performance, Form Factor and Cost”

● Two general drivers for packaging:

**Driver A):** Cost, Performance, Miniaturization
Solution: Large Scale Panel, Batch Processing
→ Wafer Level Packaging (WLCSP)

**Driver B):** More functionality on same or less space
Solution: System Integration, „More than Moore“
→ System-in-Package (SiP)

WLSiP
Enabled by FO-WLP eWLB
Value Adding Packaging

- 26k KGD chips per wafer;
- Chips size 1x1mm² and 1.2x0.8mm²;
- Resulting in total of 13k SiP;
- Package size 2x3mm².
Value Adding Packaging

- **WDoD™ = WireFree Die on Die** (patented wafer level technology by 3D-Plus)

DDR3 quad die JEDEC compatible memory modules in package
Value Adding Packaging

- eWLB wafer before RDL
- eWLB wafer DDR3 DRAM layers
- eWLB wafer bottom layer/ BGA
Value Adding Packaging

- Special eWLB Multichip Module (imaging sensor arrays for medical applications);
- 10 dies per sensor array, Package size > 900mm².
Enabler of the Enabler/Toolbox

- Building blocks inside the WLSiP enabler toolbox

- Multi-Layer RDL Development
- Discrete Passives Integration
- Mold Edge, Die-to-Die Distance Reduction
- New Dielectric Materials Introduction
- High Power Dissipation Solutions
- Reduced RDL Line/Space Development
- Thru Package Via / Double Sided RDL Development
- Package Size and Height Requirements
- Solder Ball / Pad Pitch Reduction
Enabler of the Enabler/ Toolbox

- Reduction of ball pitch aims the increase in connection density;
- Miniaturization, while increasing density of microelectronics (<40nm foundry technology node);

15um / 13um Meander Test Structure for Leakage Current measurements

- Routing ability RDL level;
- Must be followed by a correspondent reduction in RDL line/ space width (20/20 → 15/15 → 10/10).
Enabler of the Enabler/Toolbox

400µm pitch, also 4 RDL traces between pads

- Ball pad (or UBM base)
- ½ ball pad = 132.5µm
- 9 x 15µm = 135µm
- ½ ball pad = 132.5µm

L/S 15/15

320µm → 265µm
Ball pad/UBM base area reduces, which increases shear stress

20/20µm → 15/15µm
Line & Space width is reduced in order to keep same routing ability

500µm → 400µm
Ball pitch reduction

L/S 20/20

Reference: 500µm pitch, up to 4 RDL traces between pads

Reduced RDL Line/Space Development

Solder Ball / Pad Pitch Reduction
The drivers for ML-RDL are:

- Need of higher routing level (more IOs, more traces);
- Shielding needs (ground plane);
- Power dissipation needs.
Enabler of the Enabler/ Toolbox

- Test structures for leakage and contact resistance measurement

10um and 15um Leakage test structures (meander)

1st RDL

2nd RDL

Different Contact Resistance Chains
Enabler of the Enabler/ Toolbox

- To achieve the best valuable package to our customer, reduction of package form factor is mandatory;
- Benefiting from its reconstruction characteristics, eWLB can achieve outstanding reduced SiP dimensions → Capabilities for very small distances between dies and between dies and package edge w/ high accuracy).

Schematic of test vehicle for testing of reduced die-to-package-edge distance
Enabler of the Enabler/ Toolbox

- Discrete passives, besides the active dies, major component type integrated in SiP today;
- Moved from the board space around the packaged die closer to the die (inside SiP);
- Placement accuracy, component movement during and after wafer molding, interconnect behavior to the RDL was tested with good results.

0201 SMD Capacitors on reconstituted wafer
Summary & Conclusions

- eWLB applications and markets, Trend to WLSiP

Legend:
- Development/ Setup
- Available
- R&D Activities ongoing

Source: YOLE Développement, July 2012
Summary & Conclusions

- WLSiP combines system integration on package level with the advantages of large scale batch processing.
  → Consequent step to achieve the performance and cost targets of the customers.

- FO-WLP technology eWLB has the clear potential to become a technology platform for system integration on wafer level, WLSiP is becoming industrial reality.

- Toolbox development to provide the building blocks.
  → Continued design rule expansion to accommodate customer needs for new applications and markets.
  → Generation of more and more reliability data to proof technology capability is ongoing.
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  - Ana Leão (Test);
  - Oriza Tavares (Reliability).

Thank you for your attention!

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