“New perspective for bonded silicon wafers Inspection“

IR Inspection for multiple applications
Wafer Level Inspection is essential for process and equipment qualification.

Black hole for cost models

75% of Yield loss can be found here

Assumptions:
- cost/die = 1 Euro
- pack & bond = 50%
Paradigm of MEMS Production

- Short time-to-Market
- Various materials and bonding methods
- Different die sizes and functionality
- Different handling precautions
- Low Volume production

Quick and easy inspection
Wafer Inspection Methods (non Destructive)

- Infrared imaging (conventional)
  - low resolution

- Scanning Acoustic Microscopy (SAM)
  - in-water Inspection

- X-Ray
  - health & safety concerns

- „Magic mirror“
  - not suitable for deeper structures
IR Inspection Methods compared

Conventional IR Inspection

IR Inspection with Telecentric (Zoom) - Lenses
Comparison between Telecentric Lenses and Conventional Lenses

Telecentric lenses feature parallel light beams which means that the distance the photons have to travel is the same at the edge of the image and the centre of the image.

Conventional (endocentric) lenses have a perspective distortion which means all light has to pass through one single point (focal point).

MML series telecentric lens

CCTV lens, lens for a single-lens reflex
Telecentricity

With ordinary lenses, part of the surface of a subject may be hidden by asperities.

With telecentric lenses, the surface of a subject is not hidden by asperities.

Telecentric Lenses are Perfect for Measurements and recognition of shape and geometry.
Inspection in various “Depths”

Telecentric lenses usually have a very small “Depht of Field” which allows to run inspections. In the “Focal plane” only blanking out higher and deeper structures.
Application Examples

1. Void Inspection

2. Void Inspection on Highly Doped Wafers

3. Alignment Mark for multiple Wafer

4. Glass frit Sealing

5. Underfill

6. Dicing Cut
4 main causes for Voids

**Bond Quality to be inspected.**
There are several causes for the most common failure, voids

1. *Particles*
2. *outgassing*
3. *Materials properties*
4. *inappropriate handling*
Significance of Voids for 3DIC & TSV’s

3D Integrated Circuits with Through-Silicon Vias (TSVs) have significantly more severe requirements for voids than other applications of wafer bonding.

Circuits.
VOID Detection

Backside Illumination

Topside Illumination
Backside Illumination of Voids

Light is blocked by metal or dust and particles which appear dark
Topside Illumination

Light is reflected by interface layer around particles and appears appear bright
Alignment Accuracy Measurement

- Top Wafer Top & Bottom Wafer Top Surface Alignment Mark
- Top Wafer Top & Bottom Wafer Bottom Alignment Mark
Basic Principle

For High Accuracy high magnification is needed

By Image processing several images can be combined into one

By this process the Alignment mark Offset can be calculated

Z axis variation of 25μm Image merge
IR- Transmission Measurement Measurement Accuracy

- Optical Magn. 8x
- Image/Pixels Relation: 0.8 micrometer
- XY Repeatability: ± 0.2 micrometer
- System Accuracy: ± 2um
- Measurement Time: 30 Sec.
Glass Frit Bonded Wafers
Glass- frit sealing defects

Bonding Frames
Glass Frit Bonds
Seal Integrity Defect
Seal Void Defect
DICING

Dicing MEMS is much more difficult because of sensitivity of dies for:

- Contamination,
- Water & Cleaning,
- Outbreaks due to aspect ratios,
- ESD issues
Edge Dice Marks visible from

View from Wafer SIDE

Chipping is clearly visible from Top with NIR
Underfill Inspection

- Silver paste potting
- Void
- Al Frame
- Si Device
- Wire
Underfill Voids
Underfill Void
Workflow – Zoom in

8 inch Si-Au-Si

Si-Au-Si

ZOOM 1

ZOOM 2

ZOOM 3

ZOOM 4

ZOOM 5

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Wafer level IR Inspection - Conclusion

1. **Value Driver**
   Process Control; Structure Control, Integrity check

2. **Easy Operation**
   no water, lead or special handling

3. **Automated**
   Complete automated Wafer Scanning

4. **High Resolution**
   by using telecentric Zoom

5. **Versatile**
   lenses with various illuminations

IR MEMS Inspector
Halle 2, Nr. 2040
We are looking forward to supporting you even better.

Thank you!
Highly Doped Wafer Comparison SAM vs. IR-Inspector
„IR-MEMS Inspector“ vs other inspection methods

Semi Automated Inspection
Niche market
Bonding Layer By Direct Bonding - offset
MEMpax®

The Product:

- MEMpax® is a thin borosilicate glass made in the SCHOTT down-draw process
- Available in all industry standard wafer formats, e.g. 4”, 6”, 8” and 12”
- Thicknesses from 0.1 – 0.7 mm
- Target markets are the MEMS and Biotech industry

The Advantages:

- Significant cost advantage compared to polished glass wafers
- The CTE of MEMpax® is matching the CTE of silicon
- Enabling anodic bonding with silicon wafers
- Very thin wafers without grinding and polishing
- Fire-polished surface with roughness < 1nm
- Wafer formats up to 12” in thicknesses < 300µm
Example:
Comparison of production flows for a t=0.3mm wafer

**Traditional**
- Float glass (>0.7mm)
- Cut to size
- Grinding
- Polishing
- Washing
- Wafer (0.3mm)

**MEMpax®**
- Down-draw glass (0.3mm)
- Cut to size
- Wafer (0.3mm)
Installed Base
Control Software Outline 1
Control Software Outline 2

- Illumination Control
- Position Control
- Mag / FOV
- Low/High Power
- Lighting Control
- Stage Position

SCHOTT glass made of ideas
Control Software Outline 3
Control Software Outline 4

Step Movement

Designation MAG.

Movement

Magnification

Mag: 0.75
Control Software Outline 5