New Material Challenges in 32nm High-K Gate First Module

F. Graetsch, R. Carter (GLOBALFOUNDRIES)
HK Gate First Module

• 32nm Gate First High-K/Metal Gate technology is now in mass production at GLOBALFOUNDRIES FAB1 manufacturing site in Dresden, Germany.

• Presentation focus: The HK Gate First module
  – Overview on new materials and processes that were introduced in order to meet the technology requirements for high performance CMOS devices.
  – Some of the associated challenges with high-k/metal gate process integration will be discussed
Content

1. HK Gate First vs. HK Gate Last
2. Classical SiON gate module
3. HK dielectric
4. HK gate electrode
5. HK Vt setting
6. HK stack patterning
7. HK compatible wet processes
8. HK Gate First summary
# 1. HK Gate First vs. HK Gate Last

<table>
<thead>
<tr>
<th>Features</th>
<th>HK Gate First</th>
<th>Hybride HK Replacement Gate</th>
<th>Full HK Replacement Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>HK dielectric and HK metal electrode deposited in Gate Module (embedded in FEOL)</td>
<td>✔</td>
<td>✔</td>
<td>-</td>
</tr>
<tr>
<td>Workfunction materials deposited in Gate Module</td>
<td>✔</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Dummy Poly for Gate Patterning</td>
<td>-</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>Poly removal in MoL</td>
<td>-</td>
<td>-</td>
<td>✔</td>
</tr>
<tr>
<td>HK dielectric and HK metal electrode deposited in MoL</td>
<td>-</td>
<td>-</td>
<td>✔</td>
</tr>
<tr>
<td>Workfunction and fill metal deposition in MoL</td>
<td>-</td>
<td>✔</td>
<td>✔</td>
</tr>
</tbody>
</table>
2. Classical SiON gate module

1. Thick gate oxide (30-60Å thermal oxide) for higher voltage transistors
2. Resist mask and wet etch to pattern thick oxide
3. Thin gate oxide (15-20Å SiON)
4. Poly Si and Hardmask
5. Gate patterning
6. Gate reoxidation
3. HK dielectric

- HfO$_2$ vs. SiON dielectric
  - $\varepsilon \sim 25$ vs. $\varepsilon \sim 5$
  - Large gate leakage reduction
  - Enables scaling down ToxInv

- High quality interfacial oxide layer (IL)
  - Thin or thick Oxide/SiON
  - Controls ToxInv
  - Controls reliability
3. HK dielectric

- High-K/Metal Gate Benefit

For same EOT, High-K is physically thicker resulting in a gate leakage reduction (~10-100X)

→ Eliminate poly-Si depletion ($C_D$) resulting in $\Delta T_{\text{inv}} = -0.4 \text{ nm}$
3. HK dielectric challenges

• HfO$_2$ deposition
  – ALD provides excellent thickness stability
  – Proven HfCl$_4$ precursor
  – HfO$_2$ particle level matches SiON particle level

• Interfacial oxide layer formation
  – Thin IL: susceptible to reoxidation limiting ToxInv reduction
  – Thick IL: a high quality deposited oxide with properties comparable to thermal oxide
3. HK dielectric challenges

• ToxInv Control
  – IL oxide regrowth control during post-processing
  – Suppression of Vt-W effect (IL oxide regrowth under the gate at the active to field edge)

• Reliability
  – TDDB, nBTI, pBTI (new effect: O-vacancies in HfO$_{2}$)
  – Optimum thickness of IL and HfO$_{2}$ thickness
  – Optimum nitrogen dose for dielectric stack
  – Special High K anneal process
  – Moisture and oxygen control beyond standard tool capabilities for post-processing steps
4. HK gate electrode

- Metal electrode between HfO and Poly
  - Lowering ToxInv (no poly depletion)
  - Prevents Poly Fermi Pinning (Vt instability)
  - Thin TiN layer 20-50Å
  - TiN causes midgap Vt (-0.7V, +0.5V)
  - high performance devices need band edge Vt

- Poly Si or a-Si as top gate electrode
  - Uniform and defect free growth on TiN
5. HK Vt setting

• TiN needs midgap Vt correction $\sim+0.5V \rightarrow \sim+0.2V$
  $\sim-0.7V \rightarrow \sim-0.2V$

• Not possible by implant
• Achieved by workfunction (WF) adjustment
• New nFET WF material:
  – Doping of HK gate dielectric $\rightarrow$ positive fixed charge
• New pFET WF materials
  – Doping of HK gate dielectric $\rightarrow$ negative fixed charge
• New pFET channel material:
  – cSiGe deposition $\rightarrow$ valence band offset
## 5. HK Vt setting

<table>
<thead>
<tr>
<th>nWF</th>
<th>pWF</th>
<th>cSiGe</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Metal Gate (TiN)</strong></td>
<td><strong>Metal Gate (TiN)</strong></td>
<td><strong>Metal Gate (TiN)</strong></td>
</tr>
<tr>
<td>High-K (HfO$_2$)</td>
<td>High-K (HfO$_2$)</td>
<td>High-K (HfO$_2$)</td>
</tr>
<tr>
<td>Si Substrate</td>
<td>Si Substrate</td>
<td>Si Substrate</td>
</tr>
<tr>
<td>nWF capping layer (Gate First compatible)</td>
<td>HK/MG alone does not give BE Vt</td>
<td>cSiGe &amp; pWF capping layer (Gate First compatible)</td>
</tr>
<tr>
<td>nWF material (pos-charge)</td>
<td>High-K (HfO$_2$)</td>
<td>pWF material (neg-charge)</td>
</tr>
<tr>
<td>High-K (HfO$_2$)</td>
<td></td>
<td>cSiGe (VB offset)</td>
</tr>
<tr>
<td>Si Substrate</td>
<td></td>
<td>Si Substrate</td>
</tr>
</tbody>
</table>

nFET | pFET |
5. HK Vt setting challenges

• WF materials
  – Uniform and stable PVD or ALD of very thin layers
  – New metrology methods (optical, TXRF, XPS)
  – Patterning of workfunction materials
  – Low defectivity for all new processes comparable to SiON gate stack
5. HK Vt setting challenges

- Selective channel SiGe deposition
  - pWF doping does not provide enough pVt shift
  - On pFETs only, prior to interfacial oxides
  - Special hardmask scheme for cSiGe
  - Excellent cSiGe thickness control for Vt control
  - Optimization of cSiGe morphology
  - Low cSiGe defectivity
  - High productivity process (wph)
  - Thick and thin interfacial layer compatibility with cSiGe (deposited high quality oxide)
6. HK stack patterning

• Gate patterning is done with standard double patterning
• New Final Gate RIE of the High K metal gate stack with optimum gate profile across challenging topography
• ALD Nitride encapsulation to prevent IL reoxidation and TiN damage during further post-processing
7. HK compatible wet processes

- Special wet etches and cleans for WF layer patterning
- SPM, H$_3$PO$_4$ are damaging TiN electrode and were replaced by softer wet steps
- Optimized wet clean after final gate etch
- Low defectivities achieved by replacing wet bench with single wafer cleaning processes
8. HK Gate First summary

1. cSiGe hardmask patterning
2. cSiGe deposition
3. Thick IL oxide and patterning
4. Thin IL oxide and HfO$_2$ deposition
5. TiN electrode deposition incl. WF patterning
6. Poly or a-Si and Hardmask
7. Gate patterning
8. Gate encapsulation
8. HK Gate First summary
Finished devices

Source: Chipworks Technolog Blog,
October 4th, 2011, Dick James
Thank you!