Application of Silicon Interposer for 3D-Integration

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Introduction

What are major driving forces to introduce Si-Interposer?

- **Form factor**
  - Limitation of down scaling at wafer level
  - Request to increase routing and packaging density at system level

- **Mechanical stress on low-k dielectrics**
  - Stress buffer between BEoL-stacks and organic substrates

- **Electrical performance**
  - Increase of data transfer rates and band width
  - Power reduction
  - Implementation of new interfaces

- **Heterogeneous Systems**
  - Implementation of electrical and non electrical components
  - Optimization and easy replacement of single components
Silicon-Interposer for 3D Integration

Key elements of Si-Interposers

- **Substrate (Si-wafer)**
  - 300mm, standard material

- **Through Silicon Via (TSV)**
  - Oxide liner
  - Barrier and seed layer
  - Cu-metallization

- **Multi-layer wiring (RDL)**
  - Spin-on polymer for isolation
  - Cu- lines for routing

- **Contact interfaces (Bumps)**
  - Cu-stud bumps
  - Ni/Au or SnAg metallization
Silicon-Interposer for 3D Integration

Floor plan of ASSID test chip TC1.

- 3D daisy chains, integrated passives
- test structures for design verification and process optimization
Interposer Standard Process (TSV, RDL0)

**Zero Layer**
- Si-Wafer with thermal Oxide
- Application of zero layer Mask
- Oxide and Si DRIE etch
- Si-wafer with zero layer mark

**TSV-Formation**
- Application of TSV Mask
- TSV DRIE etch
- TSV wet clean, isolation, barrier/seed and ECD
- TSV –copper CMP

**RDL-Formation**
- Recess etch and top side passivation
- Open top side passivation
- Barrier/Seed and Application of RDL0 Mask
- RDL0 Plating, strip and wet etch
Interposer TSV-Process

Development Status:

- TSV-DRIE process for 20µm/100µm (AR5), 10µm/120µm (AR12) and 5µm/60µm+ (AR12+) available
- TSV-Isolation: Fabrication of oxide liner by thermal oxidation or by SA-CVD/ PE-CVD deposition
- Adhesion-/Barrier-/Seed layer: PVD deposition available up to AR12
- TSV-Fill: Cu - electrolyte with „Bottom-up“ characteristics shown for TSV with AR12
- TSV-CMP: Overburden removal with stop in oxide layer
Interposer RDL-Process

Development Status:

- Verification and alignment of initial design rules for polymer RDL and contact interfaces
- TSV/ RDL-Interfaces showing low contact resistance
- Process development and fabrication Silicon–IP with 4 layer RDL on top site and 2 layer RDL on bottom site
- Fabrication of μ-bumps (top site) and Cu-stud bumps (bottom site).
- Implementation of Cu/Ni/Au und Cu/SnAg as alternate contact metallization/ contact finish
Interposer Process: 2. Generation

Current Development Activities

- Simplification of interposer process flow by integration of RDL0-process into the TSV process

- Realization of the first level of an oxide RDL. Starting point for dual damascene process

RDL0/ TSV-Formation

- Blank Si-Wafer
- Application of RDL0 mask
- DRIE of blank Si-Wafer
- Ash RDL0 mask
- Resist Application
- Application of TSV mask and DRIE
- Isolation/Barrier/Seed TSV-Fill (Plating)
- Copper CMP/ Anneal
Interposer of the 2. Generation

Development Results

- DRIE of „RDL-cavities“ for RDL0
- Common fabrication of 1. routing layer and TSV shown
- Realization of Cu-lines and space of 3µm
- Fabrication of multi wire test structures with 5µm line width/ space

Outlook

- Development of mixed oxide/ polymer-RDL and oxide RDL
- Increase of wiring density up to 200 lines/mm
Silicon-Interposer for 3D Integration

In-Line Metrology

- X-Ray for TSV-Inspection
- Interferometer for TSV-depth measurement
- Confocal microscope for CD- and profile measurements
- Surface resistance measurements
- Layer thickness measurement (optical)
- XRF-analysis system
- Wafer bow and warp measurement
- Isolation- and leakage measurements
- Automated defect inspection
- Bump height measurement
### Outlook: RDL/TSV

#### Development Roadmap (Parameter Selection)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Standard (Current)</th>
<th>Improved (short term)</th>
<th>Advanced (mid term)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV diameter/depth</td>
<td>20µm/100µm</td>
<td>10µm/120µm</td>
<td>5µm/60µm</td>
</tr>
<tr>
<td>Line/Space: Polymer (Oxide)</td>
<td>10µm/15µm</td>
<td>8µm/10µm (5µm/5µm)</td>
<td>8µm/10µm (3µm/3µm)</td>
</tr>
<tr>
<td>ILD via: Polymer (Oxide)</td>
<td>30µm</td>
<td>20µm (10µm)</td>
<td>10µm (5µm)</td>
</tr>
<tr>
<td>Overlay: general</td>
<td>5µm</td>
<td>3µm</td>
<td>2µm</td>
</tr>
<tr>
<td>µ-bump: size/pitch/height</td>
<td>25µm/45µm/30µm</td>
<td>25µm/45µm/30µm</td>
<td>20µm/40µm/30µm</td>
</tr>
<tr>
<td>Material</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Photo resist DRIE Mask</td>
<td>10µm</td>
<td>5µm</td>
<td>3µm</td>
</tr>
<tr>
<td>Photo Resist RDL/µ-bump</td>
<td>10µm/30µm</td>
<td>5µm/40µm</td>
<td>3µm/40µm</td>
</tr>
<tr>
<td>ILD-Layer, polymer/oxide</td>
<td>5µm</td>
<td>5µm/1.5µm</td>
<td>5µm/1.0µm</td>
</tr>
<tr>
<td>TSV Isolation</td>
<td>PE-CVD oxide (1.0µm)</td>
<td>SA-CVD oxide (0.8µm)</td>
<td>Thermal Oxide (0.5µm)</td>
</tr>
<tr>
<td>TSV-Barrier</td>
<td>PVD: Ti-TiN</td>
<td>PVD: Ti-TiN /CVD: TaN-Ta</td>
<td>CVD: TaN-Ta/ Co-CVD</td>
</tr>
<tr>
<td>TSV-Seed</td>
<td>PVD: Cu</td>
<td>PVD: Cu</td>
<td>PVD: Cu/ ---</td>
</tr>
<tr>
<td>TSV-Fill</td>
<td>ECD-Cu</td>
<td>ECD-Cu</td>
<td>ECD-Cu</td>
</tr>
<tr>
<td>BS-Isolation</td>
<td>Polymer/ CVD Oxide</td>
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</tr>
<tr>
<td>Interconnects/Studs</td>
<td>Cu, Cu-SnAg, Cu-Ni-Au</td>
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</tr>
</tbody>
</table>
Outlook: TSV

- TSV-Diameter: 5 µm, 10 µm, 20 µm, 40 µm, 250 µm, 160 µm, 80 µm
- TSV-Depth: 10 µm, 20 µm, 50 µm, 100 µm, 200 µm, 400 µm, 700 µm

- Active Devices (BEOL)
- Active Devices (FEOL)
- Image Sensors
- CVD (Cu, W)
- IZM
- Interposer
- altern. via filling
- tapered TSV
- special apps
Outlook: Application

Extreme TSV:
- Fabrication of real through wafer TSV by DRIE. TSV depth of 775µm with stop on Oxide stop layer

Other Applications:
- Plasma dicing
Outlook: Silicon Interposer @ IZM-ASSID

Extension of Interposer Functionality

- Direct routing between two and more active devices
- Integration of passive devices
- Integration of active devices
- Integration of non electrical passive elements
- Integration of non electrical active elements

- Development of customized interposers
- Development of modular systems

IZM-ASSID Readiness

- Equipment 300mm wafer processing, pre-assembly and assembly,…
- Process TSV, RDL, Bumping, bonding, thinning, dicing, stacking, test
- Team experienced and motivated
Fast prototype implementation
Pilot production
Process qualification & transfer
Low volume production

Visite IZM-ASSID @ SEMICON EUROPE:
Silicon Saxony: 2.050
Fraunhofer-IZM: 1.167