3D System Integration
Technology Convergence, Progress and Challenges

Eric Beyne

the elements of innovation

11 – 13 OCTOBER  Messe Dresden, Germany

www.semiconeuropa.org
3D System Integration Technology Convergence, Progress and Challenges

Outline

• INTRODUCTION
• TSV TECHNOLOGY
• TEMPORARY CARRIER WAFER BONDING
• TEMPORARY CARRIER WAFER DE-BONDING
• CONCLUSION
Introduction:

• Characteristic for 3D-TSV System integration as emerging technology:
  – Many options
  – Complex supply chain

• Difficult for designers to actually use the technology: too many unknowns, lack of 3D-EDA

• Difficult for equipment, material and EDA tool suppliers to develop the appropriate tools and materials
Introduction

Therefore:

– Need for convergence of technology options
  ➢ Allows for convergence on design routes
  ➢ Clearly defines boundaries between supply chain partners

– Driven by applications enabled by 3D-TSV technology
3D Integration Process flow overview

IC fab: Via-middle TSV

- Si FEOL
- Cu nail
- Si BEOL

Front side bumping:

- μbumping or
- Flip chip bumping

Wafer Thinning module

- Temporary bonding to carrier
- Wafer thinning & cleaning

Backside processing

- Si recess etch
- backside passivation
- Cu TSV exposure
- Cu-RDL
- μBumping or Flip Chip bumping

Wafer debonding

3D-Stacking process

- D2D or
- Wafer level Underfill
- Wafer reconstruction

Packaging Die stack
3 Main Technology Modules for 3D TSV Integration

- TSV Technology
- Wafer thinning & Thin wafer handling
- Chip stacking & stack packaging
3D System Integration Technology Convergence, Progress and Challenges

Outline

- INTRODUCTION
- TSV TECHNOLOGY
- TEMPORARY CARRIER WAFER BONDING
- TEMPORARY CARRIER WAFER DE-BONDING
- CONCLUSION
Convergence 3D-TSV Process

IMEC’s approach: "Via-middle": fabrication TSV’s after FEOL device fabrication processing but before BEOL interconnect.

<table>
<thead>
<tr>
<th>Active Devices</th>
<th>3D-SIC/SOC</th>
<th>Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer Ø</td>
<td>300 mm</td>
<td>Baseline</td>
</tr>
<tr>
<td>TSV Ø</td>
<td>5 µm</td>
<td>3 µm</td>
</tr>
<tr>
<td>TSV depth</td>
<td>50 µm</td>
<td>50 µm</td>
</tr>
</tbody>
</table>

© IMEC 2011
3D-SIC TSV 5µm Ø, 50µm deep on 300mm

Via etch

Oxide Liner

PVD Ta/ Cu barrier seed

Cu ECD Fill

TSV anneal & CMP

Accurate Within wafer TSV depth Control

• Conformal
• Smooth surface
• Low TSV capacitance

Effective barriers: prevent Cu diffusion

Void-free bottom-up TSV-fill

• Anneal to mitigate Cu pumping
• Limited CMP dishing
3D System Integration Technology Convergence, Progress and Challenges

Outline

• INTRODUCTION
• TSV TECHNOLOGY
• TEMPORARY CARRIER WAFER BONDING
• TEMPORARY CARRIER WAFER DE-BONDING
• CONCLUSION
Thin wafer handling

• Advances in wafer thinning allow wafer thinning down to 50 µm and even less, while maintaining a total thickness variation, $TTV < 1\mu m$
• Thin wafers, below 100 µm become flexible
• Defects at the edge of the wafer cause these wafer to be fragile
Intermediate Wafer Carrier

Which Carrier solutions?

• Bonding to silicon carriers
  ➢ our preferred solution
• Bonding to glass wafers
• Bonding to perforated silicon (or glass) carriers
• Carrier-less system: grinding center wafer, leaving a narrow ridge at edge of wafer to maintain wafer shape (“Tyco”)
Requirements Temporary Bonding process

- Compatible with post processing:
- Allow for excellent thickness control (TTV) after wafer thinning on carrier
- Allow for (“low temperature” 200 - 250ºC) semiconductor processing on wafer backside:
  - Thermally stable temporary glue layer, no out gassing
  - Compatible with cassettes, loading robots, tool chucks,…
- Easy to de-bond after backside processing, preferably at low temperature without melting solder bumps
3D TSV Thinning and Backside Process flow

- Si (LSI) wafer
- Edge trim wafer
- Particle cleaning

- Si carrier wafer
- Temporary glue layer coating

- Wafer to Carrier bonding
- Wafer thinning by grinding
- Grinding damage removal (Wet/dry/CMP) and cleaning
- Thin wafer backside passivation and TSV via reveal process
- Wafer / carrier debonding clean & recycle carrier
- Dicing thin wafer on tape Particle clean

- 3D stacking
300mm Wafer Thinning performance on Si carrier wafers (16µm HT1010 glue)

Thickness variation after thinning to 50µm

TTV = 1.6µm

ISIS measurement, 1cm mesh, 1cm edge exclusion
Backside via reveal process

- Wafer thinning by Si grinding (no TSV exposure)
- Wafer backside clean and wet Si recess-etch to about 50µm final Si thickness, exposing all TSV’s with ±1 µm variation
Backside via reveal process

• Backside Wafer Passivation
• Mask-less recess etch of passivation and TSV oxide liner on top of Cu-nails: Backside contact to TSV structure

This approach effectively avoids the use of Si/Cu CMP processing (risk of Cu contamination and cost adder)
3D System Integration Technology Convergence, Progress and Challenges

Outline

• INTRODUCTION
• TSV TECHNOLOGY
• TEMPORARY CARRIER WAFER BONDING
• TEMPORARY CARRIER WAFER DE-BONDING
• CONCLUSION
Slide-Debonding of thin wafers:

- Using intermediate carrier wafer to mechanically support the thin wafer:
  - bond to thin wafer on carrier prior to debonding
  - Slide debond thin wafer + intermediate carrier
  - Clean thin wafer on this carrier (standard spin tool)
  - Debond intermediate carrier after bonding thin wafer to dicing tape

- Carrier solutions:
  - Electrostatic or vacuum wafer carriers
  - Currently: limited availability
Process window for Slide-debonding using HT1010 from Brewer science (200mm)

- Sliding speed (mm/s)
- Debond temperature (°C)
- Peak force applied (N) on 200mm wafers during debonding

Risk of glue residues

Glue shear-regime

Process window
Wafer slide-debonding Process validation

50µm thick 300mm CMOS wafer after slide debond in Suss DB12S using a monopolar electrostatic support wafer
Critical aspects slide-debonding

- Need for high temperatures is not desired in presence of solder bumps
- Sensitive (bumped) wafer surface in contact to intermediate carrier
- Limited availability of suitable intermediate carrier systems
Room-Temperature peel-debonding

– No temperature constraint with respect to solder bumps.
– The thin wafer is bonded to a dicing tape, prior to debonding:
  • The intermediate carrier (or stand-alone thin wafer handling) is not required
  • The sensitive surface of the backside of the thin wafer is protected by the dicing tape
– Preferred solution
– However:
  • New materials in development: similar low Si TTV needs to be achieved
  • Typically requires additional process steps, additional coating materials, specific tools to prepare the surfaces for peel debonding and tools for cleaning of thin wafers on tape (non-standard tools)
Thin Wafer Peel-debonding directly to Dicing Tape on Frame

50 µm thick 300mm blanket Si wafer after peel debond on tape thin wafer support in Suss DB12T
3D System Integration Technology Convergence, Progress and Challenges

Outline

- INTRODUCTION
- TSV TECHNOLOGY
- TEMPORARY CARRIER WAFER BONDING
- TEMPORARY CARRIER WAFER DE-BONDING
- CONCLUSION
Conclusions

- **3D-Integration technology** has three key components:
  - TSV technology
  - Wafer thinning and thin wafer carrier technology
  - Micro-bump interconnect technology for 3D

- *The wafer support system* is critical to the success of 3D system integration

- However it is *not yet fully mature*:
  - Limited set of materials and equipment available
  - Most temporary bonding materials still in optimization phase
ACKNOWLEDGMENT: PARTNERS
IMEC 3D SYSTEM INTEGRATION PROGRAM

Logic IDM
- Panasonic
- Intel
- Fujitsu
- Sony

Memory IDM
- Micron
- Samsung
- TSMC

Foundries
- GlobalFoundries

Fabless
- Qualcomm
- Xilinx
- Altera
- NVIDIA

EDA
- Synopsys
- Cadence
- Atrenta

OSAT
- Amkor Technology
- UTAC

Material Suppliers
- Hitachi Chemical
- Henkel
- BASF
- ThinMaterials

Equipment Suppliers
- Applied Materials
- Lam Research
- Tokyo Electron
- SCREEN
- Ultratech
- Nanda Tech
- PVA TePla
ASPIRE
INVENT
ACHIEVE